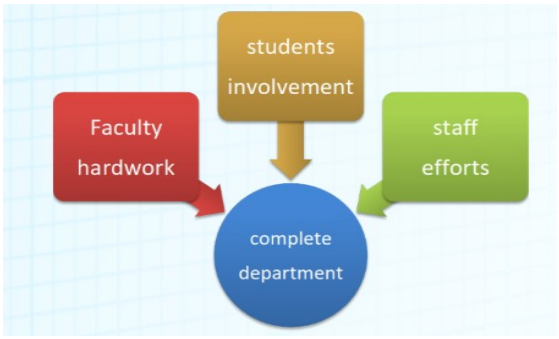
Newsletter july to September 2019

Vision

To create a centre for imparting technical education of international standards and conduct research at the cutting edge of electronics & communication technology to meet the current and future challenges of technological development.

Mission

To create technical manpower for meeting the current and future demands of industry and academia: to recognize education and research in close interaction with electronics & communication & related industry with emphasis on the development of leadership qualities in the young men and women entering the portals of the institute with sensitivity to social development and eye for opportunities for growth in the international perspective.



Seminar/Symposia/Workshop/Conference/STC Organized:

1) International Short Term Course on **GIAN courseon Principles of Bio-Photonics (Expert: Prof AlessandroM Deana, University Nove de Julho, Brazil)** at MNIT Jaipur,India from 24-06-2019 to 05-07-2019
2) National Workshop on **Antenna Trends** at MNIT Jaipur, India from 01-07-2019 to 05-07-2019
3) National Short Term Course on **VLSI chip design using open source EDA** at MNIT Jaipur, India from 08-07-2019 to 12-07-2019

4) National Workshop on **Smart Electronics Technologies and Systems** at MNIT Jaipur, India from 10-08-2019 to 14-08-2019

Publications

1) Gurjit S Walia, Ashish Kumar, Kapil Sharma, Kuldeep Singh ,"Robust Object Tracking with Crow Search Optimized Multi-cue Particle Filter" , **Pattern Analysis & Applications** Volume :0 / 1-10 / 2019

2) Arathy Varghese, Periasamy, Lava Bhargava, Surani Bin Dolmanan and SudhiranjanTripathy ,"Linear and Circular AlGaN/AlN/GaN MOS-HEMT based pH Sensor on Si Substrate: A Comparative Analysis (Accepted for Publication)" , **IEEE Sensors Letters** Volume :3 / 1-5 / 2019
3) Ashish Kumar, Mahanth Prasad, Vijay Janyani, R P Yadav ,"Design, fabrication and reliability study of piezoelectric ZnO based structure for development of MEMS acoustic sensor" , **Microsystem Technologies** Volume :0 / 0-0 / 2019 ISBN: DOI: https://doi.
4) Arathy Varghese, C. Periasamy, Lava Bhargava ,"Dielectric Modulated Underlap based AlGaN/AlN/GaN MOS-HEMT for Label Free Bio-detection " , **Nanoelectronics and Optoelectronics** Volume :2 / 1-8 / 2019
5) Arathy Varghese, C. Periasamy, and Lava Bhargava ,"Fabrication and Charge Deduction based Sensitivity Analysis of GaN MOS-HEMT Device for Glucose, MIG, c-erbB-2, KIM-1 and PSA Detection" , **IEEE Transactions on Nanotechnology (SCI: 2.857 Impact Factor)** Volume :4 / 1-8 / 2019 ISBN: 978-1-4673-0635-5
6) R. K. Vijay, S. J. Nanda ,"A Quantum Grey Wolf Optimizer based declustering model for analysis of earthquake catalogs in an ergodic framework" , **Journal of Computational Science, Elsevier** Volume :36 / 101019- / 2019 ISBN: ISSN: 1877-7503
7) Yogendra Gupta, Lava Bhargava, Ashish Sharma, MS gaur ,"Hybrid Buffers based Coarse-Grained Power Gated Network on Chip Router Microarchitecture" , **International Journal of Electronics** Volume :10 / 239-250 / 2019
8) AnkitSirohi,ChitrakantSahu,Jawar Singh ,"Analog/RF Performance Investigation of Dopingless FET for Ultra-Low Power Applications" , **IEEE ACCESS** Volume :00 / 00-00 / 2019
9) Ashish Kumar, Mahanth Prasad, Vijay Janyani and R.P Yadav ,"Fabrication and simulation of piezoelectric AlN based MEMS acoustic sensor" , **Nanoelectronics and Optoelectronics** Volume :00 / 0-0 / 2019 ISBN: IN PRESS
10) AnkurSaharia, M. Ravi Kumar, Jalil Ali, PreechaYupapin, Ghanshyam Singh ,"An elementary optical logic circuit for quantum computing: a review" , **Optical and Quantum Electronics** Volume :51 / 224 / 2019

Placement Data

Fifty four students got placed in different companies during jul-sep 2019.

Article

“New Transistor Design Aims to Surpass Moore’s Law”

Silicon integrated circuits found in computer processors, among many other devices are quickly approaching the maximum feasible density of transistors on a single chip, limiting potential design improvements for future integrated circuits. Thanks to the work of a team of engineers at the University of Michigan (U-M), however, a new approach to transistor stacking promises to solve this issue before it negatively impacts processor designers. Traditionally, transistors are constructed in a 2D configuration. This design includes an additional chip that converts between high and low voltage signals a structure that currently stands between the low voltage processing chips and the higher-voltage user interfaces.

The team from U-M (led by Becky Peterson, associate professor of electrical engineering and computer science) has stacked a second layer oftransistors directly atop a cutting-edge silicon chip 3D configuration that has eliminated the need a second chip.

Peterson’s team achieved success by utilizing a different kind of semiconductor, known as an amorphous metal oxide. To apply this semiconductor layer to the silicon chip without damaging it, they covered the chip with a solution containing zinc and tin, and then spun it to create an even coating.Following that step, the team briefly baked the chip to dry it out. This process was repeated to make a layer of zinc-tin-oxide about 75 nanometers thick (about one-thousandth the thickness of a human hair). During a final bake, the metals bonded to oxygen in the air, creating a layer of zinc-tin-oxide.
“This enables a more compact chip with more functionality than what is possible with only silicon,” said Youngbae Son, the first author of the paper and recent doctoral graduate in electrical and computer engineering at U-M. The advancements in silicon integrated chip technology established by Peterson and her team have the potential to revolutionize transistors and the methods engineers use to build complex devices—perhaps even going beyond the rate of progress dictated by Moore’s Law.