w.e.f. 17th August 2022

Dept. of ECE, MNIT Jaipur — Time Table — Odd Semester 2022-23

I Semester M. Tech. VLSI

	8-9 AM	9-10 AM	10-11 AM	11-12 PM	12-1 PM	1-2 PM	2-3 PM	3-4 PM	4-5 PM	5-6 PM
Monday		21ECT543 Dig. IC Design CP VLTC-L208	21ECT839 CAD VLSI LB VLTC-L208	21ECT544 Reduced Order Mod., opt. and Int. VS VLTC L208	21ECT541 Adv. Sem. Dev. MY VLTC-L106	Lunch	21ECT833 VLSI Sig. Proc AMJ VLTC-L106			
Tuesday			21ECT544 Reduced Order Mod., opt. and Int. VS VLTC L208	21ECT541 Adv. Sem. Dev. MY VLTC-L106	21ECT842 Dig. Sys. Des. D.Bharti VLTC-L208		PG-VLSI Sem. Device and IC Lab – 1; IC/MEMS Lab; DB, VS			
Wednesda			21ECT543 Dig. IC Design CP VLTC-L106	21ECT542 Ana. IC Design DB VLTC L208	21ECT833 VLSI Sig. Proc AMJ VLTC-L106		21ECT842 Dig. Sys. Des. D.Bharti VLTC-L208			
Thursday		21ECT543 Dig. IC Design CP VLTC-L208	21ECT839 CAD VLSI LB VLTC-L208	21ECT542 Ana. IC Design DB VLTC L208	21ECT541 Adv. Sem. Dev. MY VLTC-L106		21ECT842 Dig. Sys. Des. D.Bharti VLTC-L208			
Friday			21ECT839 CAD VLSI LB VLTC-L208	21ECT542 Ana. IC Design DB VLTC L106	21ECT833 VLSI Sig. Proc AMJ VLTC-L106					

(Dr. Bharat Choudhary) (Dr. Rajesh Saha) (Prof. Lava Bhargava)